FORM PTO-1390 (REV. 5-93)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER **10191/2235**

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

U.S. APPLICATION NO. (If known, see 37 CFR 1.5)
10/049474

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED:
PCT/DE00/02235	**08 July 2000 (08.07.00)**	**12 August 1999 (12.08.99)**

TITLE OF INVENTION
SEMICONDUCTOR ARRANGEMENT AND METHOD OF MANUFACTURE

APPLICANT(S) FOR DO/EO/US
GOEBEL, Herbert; and GOEBEL, Vesna

Applicants herewith submit to the United States Designated/Elected Office (DO/EO/US) the following items and other information.

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) immediately rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)) (unsigned).
10. ☒ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A **FIRST** preliminary amendment.
14. ☒ A substitute specification and marked-up version thereof.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information: International Search Report (translated), Preliminary Examination Report (translated) and PCT/RO/101.

EXPRESS MAIL NO.: EL594613989

U.S. APPLICATION NO. if known, see 37 C.F.R.1.5	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
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17. ☒ The following fees are submitted:

Basic National Fee (37 CFR 1.492(a)(1)-(5)):

Search Report has been prepared by the EUROPEAN PATENT OFFICE or JPO $890.00

International preliminary examination fee paid to USPTO (37 CFR 1.482) $710.00

No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) $740.00

Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO $1,040.00

International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) $100.00

	CALCULATIONS	PTO USE ONLY
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 890	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	6 - 20 =	0	X $18.00	$ 0	
Independent Claims	2 - 3 =	0	X $84.00	$ 0	
Multiple dependent claim(s) (if applicable)			+ $280.00	$	
TOTAL OF ABOVE CALCULATIONS =				$ 890	
Reduction by ½ for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28).				$	
SUBTOTAL =				$ 890	
Processing fee of $130.00 for furnishing the English translation later the ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
TOTAL NATIONAL FEE =				$ 890	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +				$	
TOTAL FEES ENCLOSED =				$ 890	
				Amount to be: refunded	$
				charged	$

a. ☐ A check in the amount of $_____ to cover the above fees is enclosed.

b. ☒ Please charge my Deposit Account No. 11-0600 in the amount of **$890.00** to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 11-0600. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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for Richard Mayer (by J. Lee Reg. No. 36,197)
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Richard L. Mayer, Reg. No. 22,490
NAME

2/12/02
DATE

[10191/2235]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	:	GOEBEL et al.
Serial No.	:	To Be Assigned
Filed	:	Herewith
For	:	SEMICONDUCTOR ARRANGEMENT AND METHOD OF MANUFACTURE
Examiner	:	To Be Assigned
Group Art Unit	:	To Be Assigned

Assistant Commissioner
for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

SIR:

Please amend the above-identified application before examination as follows:

IN THE SPECIFICATION AND ABSTRACT:

In accordance with 37 C.F.R. § 1.121(b)(3), a Substitute Specification (including the Abstract but without claims) accompanies this response. It is respectfully requested that the Substitute Specification be entered to replace the Specification of record.

IN THE CLAIMS:

Without prejudice, please cancel original claims 1-7 and cancel substitute claims 1-3. Please add new claims 8-13 as shown below:

--8. (New) A semiconductor chip comprising:

a first layer of a first conductivity type having at least two partial layers, a first

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partial layer having a first dopant concentration disposed on a second partial layer having a second dopant concentration, the second dopant concentration being less than the first dopant concentration; and

a second layer of a second conductivity type which is opposite of the first conductivity type, wherein the second layer is disposed on the first partial layer;

wherein at least one trench is provided such that the trench penetrates the first partial layer and extends into the second partial layer, and wherein the trench is covered by a continuation region of the second layer so that at least one p-n junction is provided between the second layer and the second partial layer of the chip.

9. (New) The semiconductor chip according to claim 8, wherein an edge region of the chip is beveled, and wherein additional continuation regions of the second layer are provided in the edge region to form additional p-n junctions in combination with the second partial layer.

10. (New) The semiconductor chip according to claim 8, wherein a third partial layer connected to the second partial layer is provided.

11. (New) A method for manufacturing a semiconductor chip, comprising the steps of:

providing a semiconductor wafer which includes a first layer having at least two partial layers, the first partial layer being disposed on the second partial layer, the two partial layers having a first conductivity type, the first partial layer having a first dopant concentration, the second partial layer having a second dopant concentration, and the second dopant concentration being less than the first dopant concentration;

introducing trenches into the first partial layer, which trenches extend through the first partial layer into the second partial layer;

introducing dopants of a second conductivity type into the top surface of the

wafer to change the conductivity type of a section of the first partial layer and a section of the second partial layer, whereby a second layer is formed; and

depositing metallic coatings on the top surface and the bottom surface of the wafer; and

separating the wafer along the trenches into individual chips, such that each chip has at least one trench in its interior.

12. (New) The method according to claim 11, further comprising the step of introducing the trenches by sawing.

13. (New) The method according to claim 11, further comprising the step of introducing the trenches by etching.--

Remarks

This Preliminary Amendment cancels original claims 1-7 and substitute claims 1-3 presented in the underlying PCT Application No. PCT/DE00/02235, and adds new claims 8-13. The new claims do not add new matter to the application, but do conform the claims to U.S. Patent and Trademark Office rules.

The amendments to the specification and abstract are to conform the specification and abstract to U.S. Patent and Trademark Office rules. The amendments to the specification and abstract do not introduce new matter into the application.

The underlying PCT application includes a Search Report dated December 5, 2000, and an International Preliminary Examination Report dated October 4, 2001, copies of which are submitted herewith. English translations of the Search Report and the International Preliminary Examination Report are also submitted herewith.

Applicants assert that the present invention is new, non-obvious, and useful. Consideration and allowance of the claims are requested.

Respectfully submitted,

KENYON & KENYON

Dated: February 12, 2002

By: for Richard L. Mayer (by J. Lu Reg. No. 36,197)
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chip, the allowable current load to be increased and the thermal loading of the silicon chip to be reduced in a manner that can be realized relatively simply. In so doing, a reduction in the forward voltage is simultaneously achieved. The effect of additional saw grooves is particularly advantageous, because later, when the socket and lead wire are soldered to the diode chip, the grooves lead to a better, bubble-free soldering procedure (capillary effect), and the grooves filled with solder result in additional, more effective cooling of the chip, which extends into the depth of the silicon body and therefore thermally couples the chip to the heat sink in a more effective manner.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1a shows a cross-sectional side view of a diode in accordance with the present invention.

Fig. 1b shows a plan view of the diode shown in Fig. 1a.

Fig. 2 shows a semiconductor wafer used as the starting material in a method for producing the semiconductor arrangement in accordance with the present invention.

Fig. 3 shows the semiconductor wafer in a further method step for producing the semiconductor arrangement in accordance with the present invention.

Fig. 4 shows the semiconductor wafer in yet another method step for producing the semiconductor arrangement in accordance with the present invention.

[10191/2235]

SEMICONDUCTOR ARRANGEMENT AND METHOD OF MANUFACTURE

FIELD OF THE INVENTION

The present invention relates to a semiconductor arrangement and a method for manufacturing the semiconductor arrangement.

BACKGROUND OF THE INVENTION

German Patent document No. P 4320780.4 describes a semiconductor diode having a first layer made of two partial layers, and a second layer which is situated on the first partial layer.

SUMMARY OF THE INVENTION

The present invention's semiconductor arrangement and method for manufacturing the semiconductor arrangement has the advantage of providing diodes having an increased maximum permissible power and less forward voltage for a given chip surface, in a manner suitable for large-scale mass production, without a large amount of additional engineering expense. This is particularly advantageous when a maximum preselected chip surface area should not be exceeded in order to save chip surface, and when the size of the contact socket used to contact the semiconductor arrangement should not exceed a certain magnitude, in order to avoid paying for an increased current-carrying capacity of diodes particularly used in a motor-vehicle rectifier system, with an increased volume of the entire rectifier system. The present invention facilitates, given a constant surface area of the silicon

DETAIL DESCRIPTION

Figure 1a shows a cross-sectional side view of a semiconductor chip 7, which is in the form of a diode. Chip 7 has a first semiconductor layer which is made of a first partial layer 2, a second partial layer 3, and a third partial layer 4. The doping of n-doped partial layer 2 is on the order of 10^{18} cm^{-3}. Partial layer 3 is n-doped to a concentration of approximately 10^{14} cm^{-3}, and partial layer 4 is doped to an - concentration of approximately 10^{20} cm^{-3}. Two trenches 10 are introduced into partial layer 2, which trenches extend into partial layer 3. These trenches 10 are situated in inner region 13 of chip 7. Edge regions 12 of the chip have a bevel 11, which extends into partial layer 3 as do trenches 10. Deposited onto first partial layer 2, both into trenches 10 and in bevel 11, is a second layer 20, whose regions in trenches 10 and bevels 11 are designated as continuation regions 23 and further continuation regions 24 of second layer 20, respectively. Second layer 20 is p-doped and has a doping on the order of 10^{20} cm^{-3}. The wafer topside, which is covered by layer 20, and the wafer bottom side, which is formed by layer 4, are provided with metallic coatings 22 and 21, respectively. Figure 1b shows a plan view of the chip 7 shown in Figure 1a. The top of chip 7 is covered by metallic coating 22. As a result of the trenches 10 that are introduced, this metallic coating 22 has a pattern characterized by corresponding depressions.

The p-n junction region of the diode is formed by p-doped layer 20 and n-doped layers 2 and 3 of Figure 1a. As a result of the trenches 10 that are introduced, continuation regions 23 in interior 13 of chip 7 form a p-n junction with second

partial layer 3. These regions lead to a reduction in the forward voltage of the diode, with metallic coating 22 being used as the anode and metallic coating 21 being used as the cathode. The four grooves in the interior of chip 7 (cf. Figure 1b) allow the electrical load to be increased by over 12% in comparison with an identically constructed diode not having grooves in the interior. In other words, a diode that can withstand, for example, a 65 A load may be converted to a diode having a maximum load of 75 A. An 80 A diode becomes a 90 A diode. The forward voltage may be reduced by approximately 60 mV (measured at a 100 A load). The four additional grooves or trenches in the interior of chip 7 also result in the chip being soldered more effectively and free of bubbles, i.e. the socket and lead wire are attached to the diode chip in an improved manner. In addition, the grooves filled with solder during this soldering procedure (not shown in the figure) ensure that the chip cools in an improved manner, since the solder in the grooves, which then completely fills the grooves, thermally couples the chip in an intensive manner, to a metal base used as a heat sink.

Figure 1b shows an exemplary embodiment of a chip 7, i.e., a square chip. However, not only are squares possible, but also other surfaces that are defined by straight edges (e.g. a hexagon or an octagon) and have additional, corresponding internal grooves parallel to the edges.

Figure 2 shows a semiconductor wafer having a first partial layer 2, a second partial layer 3, and a third partial layer 4, which wafer is used in producing the semiconductor arrangement of the present invention. All three partial layers are n-doped. The starting point for manufacturing this

sequence of layers is a weakly n-doped wafer, whose dopant concentration corresponds to the dopant concentration of partial layer 3. N-dopant, e.g. phosphorus, is then introduced onto and diffused into the topside and bottom side, using film diffusion. A layer, whose dopant concentration corresponds to partial layer 2, is consequently formed on the topside, and a layer, whose dopant concentration corresponds to partial layer 4, is formed on the bottom side. In this context, the dopant concentration of the layers is determined by the dopant concentration of the films.

The manufacture of such a layer sequence is already known from German Patent document No. P 4320780.4. As an alternative, this sequence of layers can also be manufactured using neutral films, as is described in the German patent application No. 19857243.3.

Figure 3 shows a further step of the manufacturing method for producing the semiconductor arrangement according to the present invention. In this context, trenches 10 are introduced into the semiconductor wafer, which subdivide partial layer 2 into subsections, trenches 10 extending through to partial layer 3. Trenches 10 can be introduced, for example, by sawing or etching. The spacing of trenches 10 is adjusted in such a manner that the wafer can subsequently be separated along the trenches, into individual chips; after the separation, each chip still has at least one trench 10 in its interior. However, the wafer surface is first cleaned prior to being processed further, in order to remove any remaining particles from the surface.

In comparison with the device and method described in German Patent document P 4320780.4, the spacing of the saw lines is halved during the sawing-in procedure (in order to obtain two additional grooves per chip) or reduced to one third (in order to obtain four additional grooves per chip). In the present case, the spacing of the grooves is typically 1-3 mm. No additional method step is necessary here, since, as is known from German Patent document P 4320780.4, the sawing-in procedure is executed to lay out the chip edge, anyway. One must only set the line spacing to be somewhat small er during the sawing-in procedure. This does not considerably change the processing time of this sawing step, since the wafer handling, the alignment, and the cleaning with deionized water done in the automatic sawing device after the sawing-in procedure, are carried out anyway.

After the introduction of trenches 10, a p-dopant such as Boron is introduced into the topside. At the same time, the dopant concentration of bottom layer 4 may be increased if so desired. P-dopant is introduced again, using film diffusion. In this diffusion step, possible defects present in the silicon monocrystal in the immediate vicinity of trenches 10 are repaired. The p-diffusion converts the top layer of the silicon wafer into a p-conductive region. The thickness of this p-layer is approximately uniform over the length of the device, even in the trenches. In Figure 4, the resulting p-conductive layer is represented by reference numeral 20. Subsequent to the deposition of layer 20 and the possible intensification of the doping of partial layer 4, the two sides of the wafer are metallized so that p-conductive layer 20 is provided with a metallic coating 22 and n-doped, third partial layer 4 is provided with a metallic coating 21. In a

further step, the wafer is diced along separation lines 25, into a plurality of individual diodes, so that individual chips 7 are formed whose structure is described in Figures 1a and 1b. Prior to sawing the wafer along separation lines 25, the wafer side having metallic coating 21, i.e. the bottom side, is pasted to a sawing sheet so that the individual chips do not fly off in an uncontrolled manner or become damaged.

The width of the saw lines during the sawing-in procedure is approximately 40 to 150 μm, and the lengths of the chip edges are in the range of approximately 5 mm. The area of the additional saw grooves in the interior of the individual chips only makes up a few percent of the chip surface. Of course, the method of the present invention can also be used to manufacture diodes doped in an opposite manner, i.e. diodes where a p-doped wafer is used as a starting point, in place of an n-doped wafer.

Abstract

A semiconductor arrangement and a method for manufacturing the semiconductor arrangement are provided, which arrangement and method allow an improvement in the current-carrying capacity for given chip dimensions. The semiconductor arrangement includes trenches introduced in the interior of the chip, which trenches reduce power loss and improve the heat dissipation of the chip, as well as reduce the forward voltage of diode.

[10191/2235]

SEMICONDUCTOR ARRANGEMENT AND METHOD OF MANUFACTURE

Background Information

The present invention starts out from a semiconductor arrangement and a method for manufacturing the semiconductor arrangement according to the species defined in the independent claims. German Patent Application No. P 4320780.4 describes a semiconductor diode having a first layer made of two partial layers, and a second layer, where the second layer is situated on the first partial layer.

Summary of the Invention

In contrast, the present invention's semiconductor arrangement and method for manufacturing the semiconductor arrangement, which include the characterizing features of the independent claims, have the advantage of providing diodes having an increased maximum permissible power and less forward voltage, given a constant chip surface, in a manner suitable for large-scale mass production, without a large amount of additional engineering expense. This is particularly advantageous, when a maximum preselected chip surface area should not be exceeded in order to save chip surface, and when the size of the contact socket used to contact the semiconductor arrangement should not exceed a certain magnitude, in order to avoid paying for an increased current-carrying capacity of diodes particularly used in a motor-vehicle rectifier system, with an increased volume of the entire rectifier system. Therefore, the present invention shows how, given a constant surface area of the silicon chip, the allowable current load can be increased and the thermal loading of the silicon chip can be reduced in a manner whose technology can be realized relatively simply. In so doing, a reduction in the forward voltage is simultaneously achieved.

The effect of additional saw grooves proves to be particularly advantageous, because later, when the socket and lead wire are soldered to the diode chip, the grooves lead to a better, bubble-free soldering procedure (capillary effect), and the grooves filled with solder result in additional, more effective cooling of the chip, which extends into the depth of the silicon body and therefore thermally couples the chip to the heat sink in a more intensive manner.

Additional advantages result from the further refinements specified in the dependent claims, as well as from improvements to the semiconductor arrangement and method indicated in the independent claims.

Brief Description of the Drawing

Exemplary embodiments of the present invention are shown in the drawings and explained in detail in the following description.

The figures show:

Figure 1a	a cross-sectional side view of a diode;
Figure 1b	a plan view of a diode;
Figure 2	a method step; and
Figures 3 and 4	further method steps.

Description of the Exemplary Embodiments

Figure 1a shows a cross-sectional side view of a semiconductor chip 7, which is in the form of a diode. Chip 7 has a first semiconductor layer (2, 3, 4), which is made of a first partial layer 2, a second partial layer 3, and a third partial layer 4. The doping of n-doped partial layer 2 is on the order of 10^{18} cm^{-3}. Partial layer 3 is n-doped to a concentration of

approximately 10^{14} cm^{-3}, and partial layer 4 is doped to an - concentration of approximately 10^{20} cm^{-3}. Two trenches 10 are introduced into partial layer 2, which extend into partial layer 3. These trenches 10 are situated in inner region 13 of chip 7. Edge regions 12 of the chip have a bevel 11, which extends into partial layer 3 as do trenches 10. Deposited onto first partial layer 2, both into trenches 10 and in bevel 11, is a second layer 20, whose regions in trenches 10 and bevels 11 are designated as continuation regions 23 and further continuation regions 24 of second layer 20, respectively. Second layer 20 is p-doped and has a doping on the order of 10^{20} cm^{-3}. The wafer topside, which is covered by layer 20, and the wafer bottom side, which is formed by layer 4, are provided with metallic coatings 22 and 21, respectively. Figure 1b shows a plan view of the same component. The top of chip 7 is covered by metallic coating 22. As a result of the trenches 10 that are introduced, this metallic coating 22 has a pattern characterized by corresponding depressions.

The p-n junction region of the diode is formed by p-doped layer 20 and n-doped layers 2 and 3. As a result of the trenches 10 that are introduced, continuation regions 23 in interior 13 of chip 7 form a p-n junction with second partial layer 3. These regions lead to a reduction in the forward voltage of the diode, with metallic coating 22 being used as the anode and metallic coating 21 being used as the cathode. The four grooves in the interior of chip 7 (cf. Figure 1b) allow the electrical load to be increased by over 12% in comparison with an identically constructed diode not having grooves in the interior. In other words, a diode that can withstand, for example, a 65 A load may be converted to a diode having a maximum load of 75 A. An 80 A diode becomes a 90 A diode. The forward voltage may be reduced by approximately 60 mV (measured at a 100 A load). The four additional grooves or trenches in the interior of chip 7 also

result in the chip being soldered more effectively and free of bubbles, i.e. the socket and lead wire are attached to the diode chip in an improved manner. In addition, the grooves filled with solder during this soldering procedure (not shown in the figure) ensure that the chip cools in an improved manner, since the solder in the grooves, which then completely fills the grooves, thermally couples the chip in an intensive manner, to a metal base used as a heat sink.

Figure 1b represents the special case of a square chip 7. However, not only are squares possible, but also other surfaces that are defined by straight edges (e.g. a hexagon or an octagon) and have additional, corresponding, internal grooves parallel to the edges.

Figure 2 shows a semiconductor wafer having a first partial layer 2, a second partial layer 3, and a third partial layer 4. All three partial layers are n-doped. The starting point for manufacturing this sequence of layers is a weakly n-doped wafer, whose dopant concentration corresponds to the dopant concentration of partial layer 3. N-dopant, e.g. phosphorus, is then introduced onto and diffused into the topside and bottom side, using film diffusion. A layer, whose dopant concentration corresponds to partial layer 2, is consequently formed on the topside, and a layer, whose dopant concentration corresponds to partial layer 4, is formed on the bottom side. In this context, the dopant concentration of the layers is determined by the dopant concentration of the films.

The manufacture of such a layer sequence is already known from German Patent Application No. P 4320780.4. As an alternative, this sequence of layers can also be manufactured using neutral films, as is described in the German patent application having the number 19857243.3.

Figure 3 shows a further step of the manufacturing method according to the present invention. In this context, trenches 10 are introduced into the semiconductor wafer, which subdivide partial layer 2 into subsections, trenches 10 extending through to partial layer 3. Trenches 10 can be introduced, for example, by sawing or etching them. The spacing of trenches 10 is adjusted in such a manner, that the wafer can subsequently be separated along the trenches, into individual chips; after the separation, each chip still having at least one trench 10 in its interior. However, the wafer surface is first cleaned prior to being processed further, in order to remove any possibly remaining particles from the surface.

In comparison with German Patent Application P 4320780.4, the spacing of the saw lines is halved during the sawing-in procedure (in order to obtain two additional grooves per chip) or reduced to one third (in order to obtain four additional grooves per chip). In this case, the spacing of the grooves is typically 1-3 mm. No additional method step is necessary here, since, as is known from P 4320780.4, the sawing-in procedure is executed to lay out the chip edge, anyway. One must only set the line spacing to be somewhat smaller during the sawing-in procedure. This does not considerably change the processing time of this sawing step, since the wafer handling, the alignment, and the cleaning with deionized water done in the automatic sawing device after the sawing-in procedure, are carried out anyway.

After the introduction of trenches 10, a p-dopant such as Boron is introduced into the topside. At the same time, the dopant concentration of bottom layer 4 can be increased if this appears to be advantageous. P-dopant is introduced again, using film diffusion. In this diffusion step, possible defects present in the silicon monocrystal in the immediate vicinity

of trenches 10 are repaired. The p-diffusion converts the top layer of the silicon wafer into a p-conductive region. The thickness of this p-layer is approximately uniform over the surface, even in the trenches. In Figure 4, the resulting p-conductive layer is represented by reference numeral 20. Subsequent to the deposition of layer 20 and the possible intensification of the doping of partial layer 4, the two sides of the wafer are metallized so that p-conductive layer 20 is provided with a metallic coating 22 and n-doped, third partial layer 4 is provided with a metallic coating 21. In a further step, the wafer is diced along separation lines 25, into a plurality of individual diodes, so that individual chips 7 are formed whose structure is described in Figures 1a and 1b. Prior to sawing the wafer along separation lines 25, the wafer side having metallic coating 21, i.e. the bottom side, is pasted to a sawing sheet so that the individual chips do not fly off in an uncontrolled manner or become damaged.

The width of the saw lines during the sawing-in procedure is approximately 40 to 150 μm, and the lengths of the chip edges are in the range of approximately 5 mm. The area of the additional saw grooves in the interior of the individual chips only makes up a few percent of the chip surface. Of course, the method of the present invention can also be used to manufacture diodes doped in an opposite manner, i.e. diodes where a p-doped wafer is used as a starting point, in place of an n-doped wafer.

What is claimed is:

1. A semiconductor arrangement, in particular a diode, which takes the form of a chip (7) and has a first layer (2, 3, 4) of a first conductivity type and a second layer (20) of the opposite conductivity type; the first layer being made of at least two partial layers (2, 3), the first partial layer (2) having a first dopant concentration and the second partial layer (3) having a second dopant concentration, the second dopant concentration being less than the first, the second layer (20) being situated on the first partial layer (2), and the first partial layer (2) being situated on the second partial layer (3); wherein at least one trench (10) is introduced in the inner region (13) of the chip; the trench penetrating the first partial layer and extending to the second partial layer, and the trench being covered by a continuation region (23) of the second layer (20), so that at least one p-n junction is between the second layer (20) and the second partial layer (3), in the interior of the chip.

2. The semiconductor arrangement as recited in Claim 1, wherein the edge region (12) is beveled, so that further continuation regions (24) of the second layer, which are situated in the edge region, form additional p-n junctions together with the second partial layer.

3. The semiconductor arrangement as recited in Claim 1 or 2, wherein a third partial layer (4) is provided, which is connected to the second partial layer.

4. The semiconductor arrangement as recited in Claim 3, wherein a metallic coating (22) is provided, which is joined to the second layer, and an additional metallic coating (21) is provided, which is joined to the third

partial layer; and the concentrations of the second layer and the third partial layer are selected so as to ensure an ohmic contact between the second layer and the third partial layer, and the respective metallic coatings.

5. A method for manufacturing a semiconductor arrangement, where

in a first step, a semiconductor wafer (1) is provided, which includes a first layer (2, 3) having at least two partial layers, the first partial layer (2) being deposited on the second partial layer (3), the two partial layers being of a first conductivity type, the first partial layer having a first dopant concentration, the second partial layer having a second dopant concentration, and the second dopant concentration being less than the first;

in a further step, trenches (10) are introduced into the first layer, which extend through the first partial layer into the second partial layer;

in a further step, dopants of the opposite conductivity type are introduced into the topside of the wafer to change the conductivity type of a section of the first partial layer and a section of the second partial layer, in order to form a second layer (20); and

in a further step, metallic coatings (21, 22) are deposited on the topside and the bottom side of the wafer;

wherein, in a further step, the wafer is separated along the trenches, into individual chips, in such a manner, that each chip has at least one trench (10) in its

interior.

6. The method as recited in Claim 5, wherein the trenches are introduced by sawing them.

7. The method as recited in Claim 5, wherein the trenches are introduced by etching them.

Abstract

Proposed is a semiconductor arrangement and a method for manufacturing the semiconductor arrangement, which allow an improvement in the current-carrying capacity for given chip dimensions. The semiconductor arrangement includes trenches introduced in the interior of the chip, in order to reduce power loss and improve the heat dissipation of the chip.

(Figure 1a)

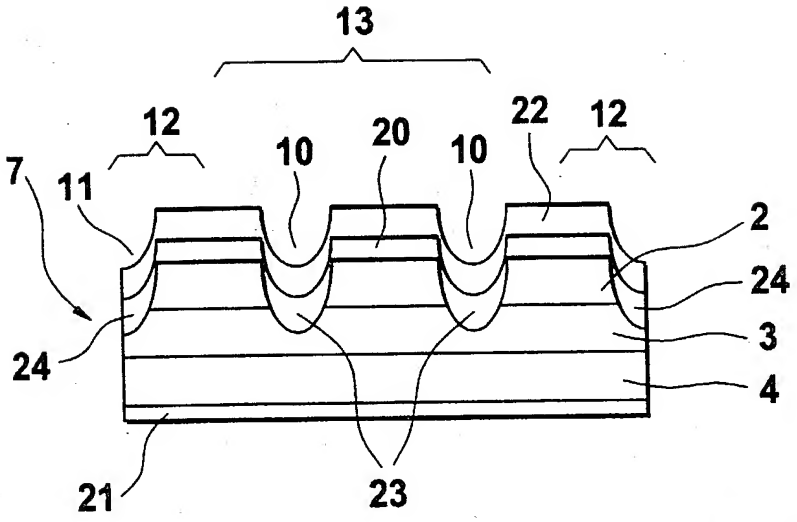

Fig. 1a

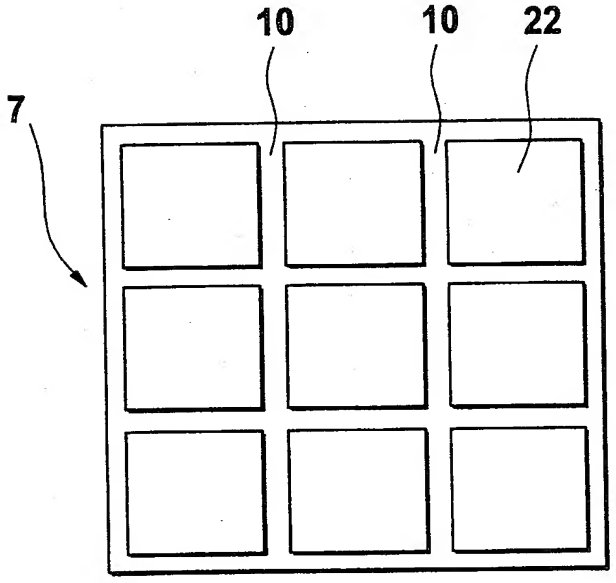

Fig. 1b

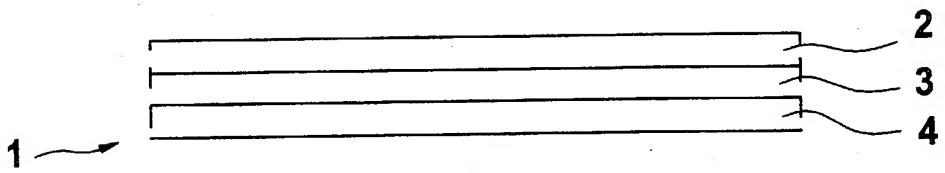

Fig. 2

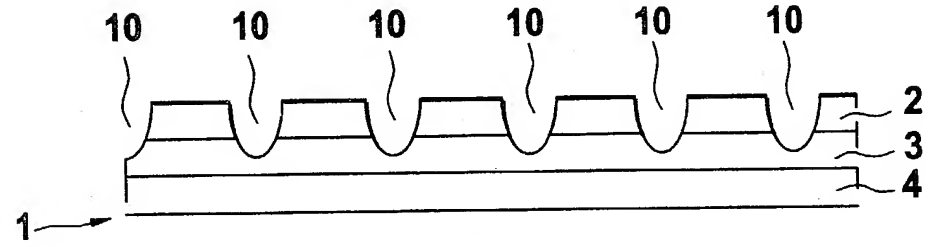

Fig. 3

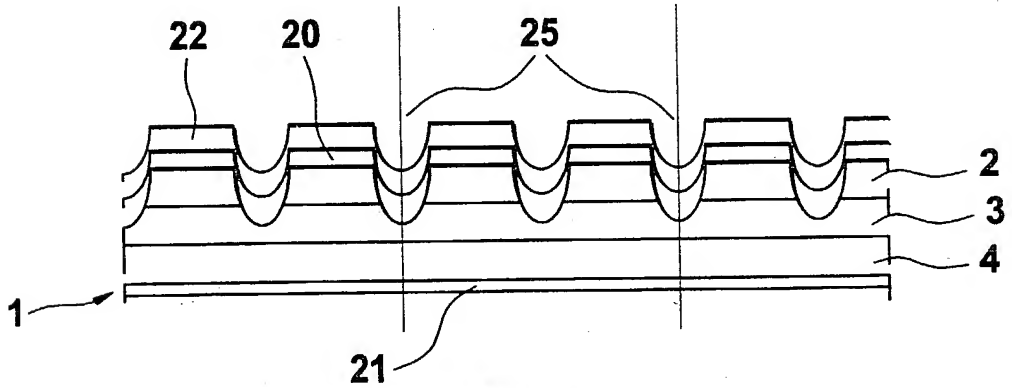

Fig. 4

PRIOR FOREIGN/PCT APPLICATION(S)
AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. § 119

Country : Federal Republic of Germany

Application No. : 199 38 209.3

Date of Filing: 12 August, 1999

Priority Claimed
Under 35 U.S.C. § 119 : [x] Yes [ ] No

I hereby claim the benefit under Title 35, United States Code § 120 of any United States Application or PCT International Application designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations § 1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application:

PRIOR U.S. APPLICATIONS OR
PCT INTERNATIONAL APPLICATIONS
DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. § 120

U.S. APPLICATIONS

Number :

Filing Date :

PCT APPLICATIONS
DESIGNATING THE U.S.

PCT Number :

PCT Filing Date :

10191/2235

COMBINED DECLARATION AND
POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled **SEMICONDUCTOR ARRANGEMENT AND METHOD OF MANUFACTURE**, and the specification of which:

[ ] is attached hereto;

[ ] was filed as United States Application Serial No. _____ on _____, 19__ and was amended by the Preliminary Amendment filed on _____, 19__.

[x] was filed as PCT International Application Number PCT/DE00/02235, on the 8th day of July, 2000.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a). I hereby claim foreign priority benefits under Title 35, United States Code § 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international applications(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

EL594613989

I hereby appoint the following attorney(s) and/or agents to prosecute the above-identified application and transact all business in the Patent and Trademark Office connected therewith.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

1-e

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